UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/903,453	07/29/97	FORBES	L 303.378US1

MMC2/0522
SCHWEGMAN LUNDBERG WOESSNER & KLUTH
PO BOX 2938
MINNEAPOLIS MN 55402

EXAMINER	
ECKERT II,G	
ART UNIT	PAPER NUMBER
2815	

DATE MAILED:
05/22/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/903,453	Forbes et al.
Examiner	**Art Unit**
George C. Eckert II	2815

– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Feb 23, 2001*

2a)☒ This action is **FINAL.** 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 20-68* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideratio

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 20-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some* c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)

16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *25*

18)☐ Interview Summary (PTO-413) Paper No(s). _____

19)☐ Notice of Informal Patent Application (PTO-152)

20)☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's amendment in which claims 1-5, 20, 21, 24, 29, 31, 32, 35, 36, 38-48 and 50-64 and claims 65-68 newly added has been entered of record.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b). **Claims 1-6 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18 of co-pending Application No. 08/902,843.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 68 is rejected under 35 U.S.C. 102(a) as being anticipated by JP 08-255878 to Sugita et al. Sugita et al. teach, with reference to figure 3 and the English abstract, a transistor comprising:

a source region (2) in a substrate (1);

a drain region (3) in the substrate (1);

a channel region (inherent between a source and drain) between the source region and the drain region in the substrate;

a floating gate (6); and

means 5 for separating the floating gate from the channel region.

4. Claims 4, 5, 20, 23, 29, 32 and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by, or, in the alternative, obvious over Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures*, Electronics Letters, April 28, 1994, Vol. 30, No. 9 (of record).

With regard to claim 4, Sakata et al. teach in figure 1, a capacitive device comprising:

a first conductor layer shown as the a-Si:H layer which is supported by a silicon substrate which is taught to be doped and therefore semiconducting;

a dielectric layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed on top of the first conductor layer; and

a second conductor layer shown as metal and formed on top of the dielectric layer.

With regard to claim 5, Sakata et al. teach that the layers extend substantially vertically from a general surface of the substrate. With regard to claim 20, Sakata et al. teach that the device may be used in a floating gate memory device (last paragraph in first column on page 688) wherein the a-Si:H layer is a floating gate and a layer of amorphous silicon carbide is between the floating gate and the substrate. With regard to claim 23, Sakata et al. teach under *Sample preparation* that the substrate is crystalline silicon doped n- or p-type. With regard to claims 29, 32 and 36, Sakata et al. teach the first conductive layer of a-Si:H supported by the substrate, the

layer of amorphous SiC:H there over, and a second conductive layer of metal over the layer of a-SiC:H. The different intended uses cited in the preambles of these claims are not sufficient to establish patentability over that taught by Sakata et al., since the device of Sakata et al. is a semiconductor device which may be used as a memory cell and is inherently capacitive.

Regarding the amended language as to the process by which the instant invention is formed, Applicant's have included in claims 4, 20, 29, 32 and 36 the limitation that the amorphous carburized silicon is *grown* on the substrate. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation of instant claims 4, 20, 23, 29, 32 and 36.

In the alternative, and with further regard to claim 5 (where the *growth* process is further limited to be a microwave PECVD), limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the

process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a 102/103 rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46, 50 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. With regard to these claims and as discussed above, Sakata et al. have taught the structure of a floating gate device having a doped monocrystalline silicon substrate, a graded amorphous silicon carbide layer thereon, an amorphous silicon layer to serve as a floating gate, a second amorphous silicon carbide layer thereon, and a metal layer to serve as a control gate. Sakata et al. do not expressly disclose the device comprising source, drain or channel regions. However, because Sakata et al. do teach that the device can be applied as a memory device, specifically a floating gate device, these features

are considered obvious. Sakata et al. further state on page 689 that the device can be used as a dynamic random access memory (DRAM). Both a floating gate device (typically used as an erasable programmable read only memory device or EPROM) and a DRAM device comprise source/drain and channel regions to effect a transistor capable of memory functions. Also, it is well known in the art that appropriate circuitry such as word lines and bit lines are required to effect a memory array.

Regarding the limitations that the substrate comprises a semiconductor surface layer on an underlying insulating portion, such limitation is also considered obvious. Placing a semiconducting layer on an underlying insulating layer results in a device commonly referred to as silicon-on-insulator (SOI). By placing the semiconducting layer above an insulator, several advantages are realized. SOI reduces capacitive coupling between various circuit elements over the entire IC chip, reduces chip size and/or increases packing density, and minimum device separation is determined only by the limitations of lithography. Therefore the claimed limitations that the device be formed over an underlying insulating portion are also considered obvious changes over that taught by Sakata et al.

Regarding, the limitations that the substrate is p-type while the source and drain regions are n-type, are considered obvious over that taught by Sakata et al. First, Sakata et al. teach that the substrate may be formed having a p-type conductivity (see column 2, under *Sample preparation*). As such, because it is well known that a transistor formed in a p-type substrate

will also be formed with n-type source/drain regions (to form an NMOS transistor), those limitations in the instant claims are considered obvious.

Finally, regarding the amended language as to the process by which the instant invention is formed, Applicant's have included in claims 1-3, 24, 29, 45, 46 and 50 the limitation that the amorphous carburized silicon is *grown* on the substrate. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation of instant claims 1-3, 24, 29, 45, 46 and 50.

In the alternative, and with further regard to claim 21, 39, 41, 44 and 65 (where the *growth* process is further limited to be a microwave PECVD), limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a

product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

6. Claims 31, 35, 38, 40, 42, 43, 47-49, 51-64, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al. as applied above, and further in view of Sugita et al. (of record). Sakata et al. taught the device of claims 1, 2, 3, 21, 29, 32, 36, 46 and 50 as discussed above. However, the device was not taught wherein the conductive layers which constitute the floating and control gates comprise polysilicon. Sugita et al. teaches a device using a silicon carbide insulator wherein the floating gate 6 is polysilicon. Polysilicon is well known as a gate conductor in the art. Its use as the control gate electrode is considered an obvious change over that taught by Sakata et al., especially in light of the use of polysilicon as a floating gate as taught by Sugita et al.

Regarding the amended language as to the process by which the instant invention is formed, Applicant's have included in claims 48, 52, 53, 57, 61 and 63 the limitation that the amorphous carburized silicon is *grown* on the substrate. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation of instant claims

In the alternative, and with further regard to claim 31, 35, 38, 40, 42, 43, 47, 51, 54-56, 58-60, 62, 64, 66 and 67 (where the *growth* process is further limited to be a microwave PECVD), limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Sakata et al. and Sugita et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the polysilicon as taught by Sugita et al. in the device of Sakata et al. The

motivation for doing so is that polysilicon is a well known conductor in the art as established by Sugita et al. Therefore, it would have been obvious to combine Sakata et al. with Sugita et al. to obtain the invention of claims 31, 35, 38, 40, 42, 43, 47-49 and 51-64.

Response to Arguments

7. Applicant's arguments filed February 23, 2001 have been fully considered but they are not persuasive. With regard to the double patenting rejection, because the instant claims are not considered allowable, the rejection is maintained. Regarding the rejections under §102, applicant argues that the instant claims are patentable based on the inclusion of a processing limitation. Specifically because the layer of amorphous silicon carbide of the instant device is *grown* whereas the layer of Sakata et al. is *deposited.* First, and as explained in the rejection above, it is not established that a growth process is different from a deposition process. Second, if there *is* a difference in the two processes such that the final structure of applicant's invention is *physically* or *structurally* different, the burden is on applicant to establish such difference. And because such difference has not been established, the rejection is proper.

Regarding the rejections under §103, applicant first argues as to the process by which the amorphous silicon carbide was formed. However, as discussed immediately above and in the rejections, such arguments are not convincing as they are drawn to a product by process. Applicant also argues that the rejection is improper as it did not establish a teaching or motivation to combine a source, drain or channel with the disclosure of Sakata et al. However,

this argument is without merit because the rejection clearly indicates where Sakata et al. do suggest such additional structure.

Applicant again makes arguments to the method by which the instant device is made and the limitations drawn to such method. Again however, such process limitations carry little weight absent some showing by the applicant that the final *structure* is different than that taught by the reference. And again, because no evidence was provided, the rejection is proper and the argument is not convincing. Finally, applicant argues that the combination of Sakata et al. with Sugita et al. fails as no motivation was shown for the combination of the two references. However, motivation was established in the above rejection in that polysilicon is a well known conductor, ubiquitous in the field. As such, the argument is not found persuasive.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
May 19, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800